FIG. 1

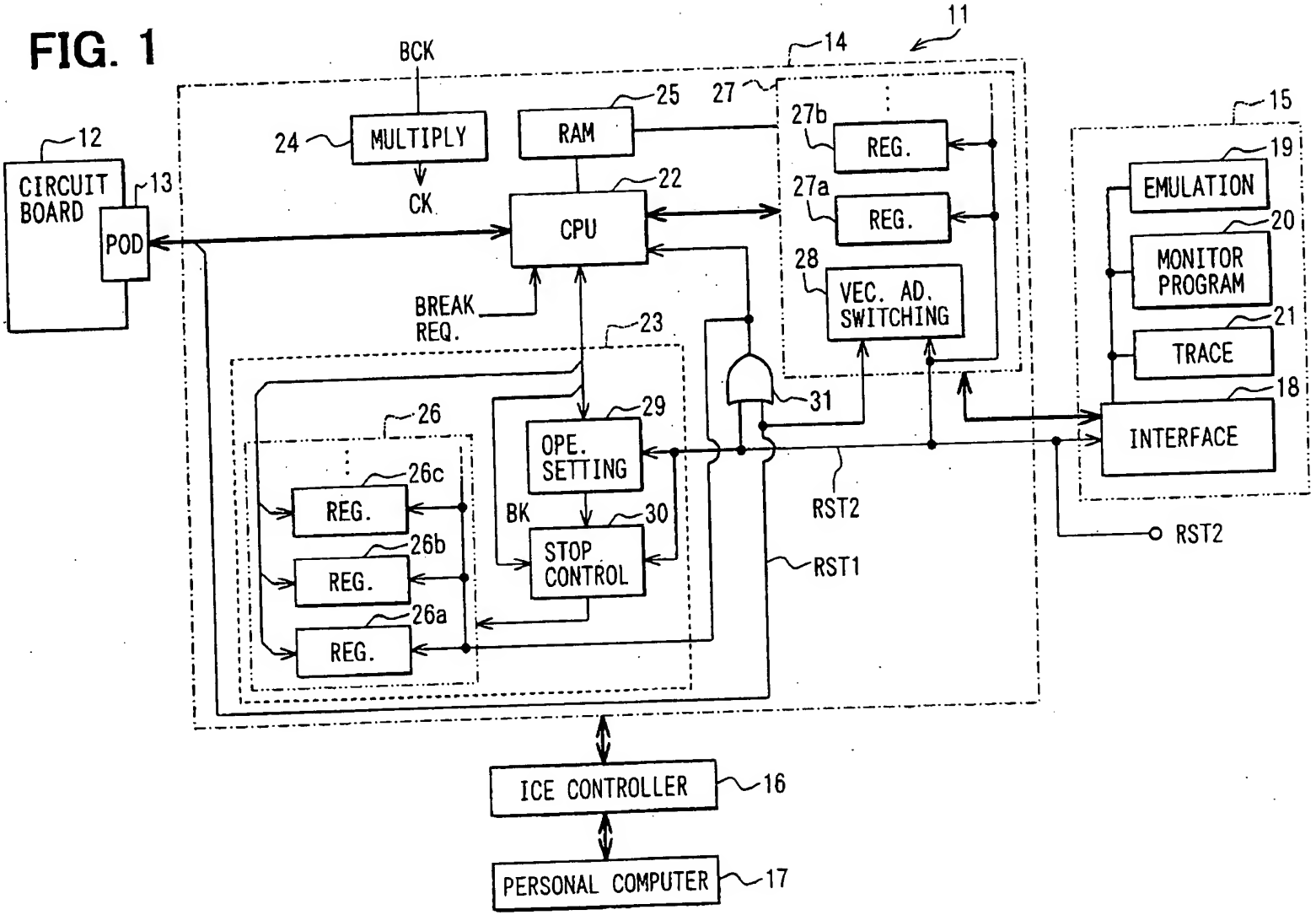

11
BCK
14
25
27
15
12
24
MULTIPLY
RAM
27b
REG.
19
CIRCUIT BOARD
13
CK
22
27a
REG.
EMULATION
20
POD
CPU
28
VEC. AD. SWITCHING
MONITOR PROGRAM
BREAK REQ.
23
21
TRACE
18
31
26
29
INTERFACE
OPE. SETTING
26c
REG.
BK
30
RST2
RST2
26b
REG.
STOP CONTROL
RST1
26a
REG.
ICE CONTROLLER
16
PERSONAL COMPUTER
17

FIG. 2A

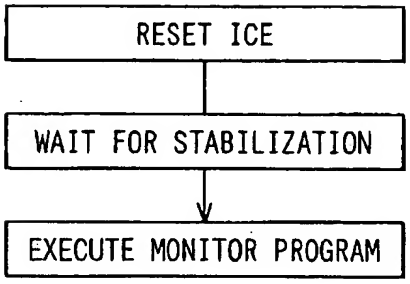


FIG. 2B

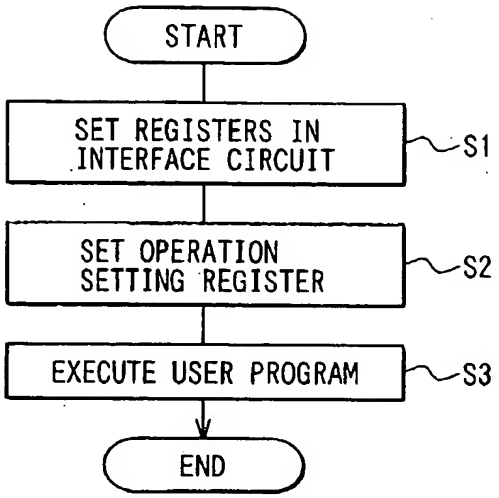


FIG. 3A

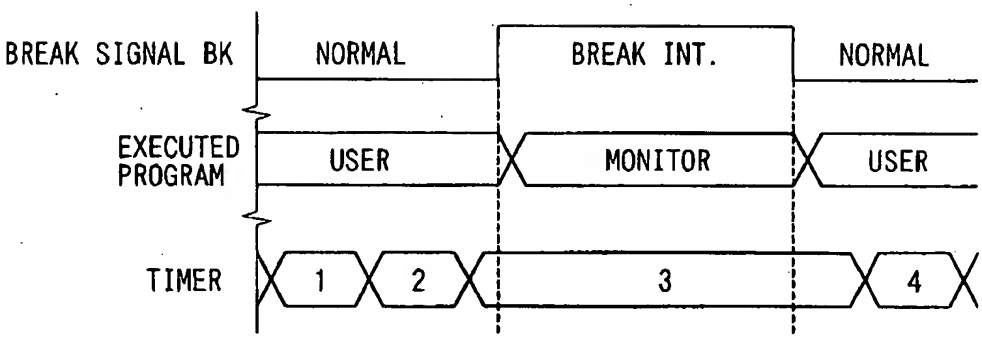


FIG. 3B PRIOR ART

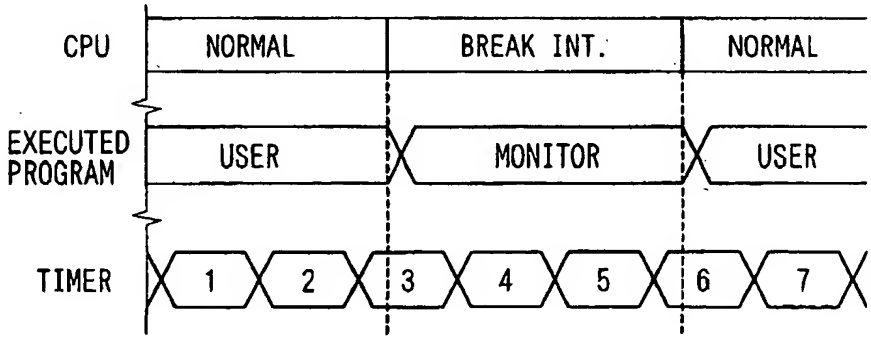


FIG. 4

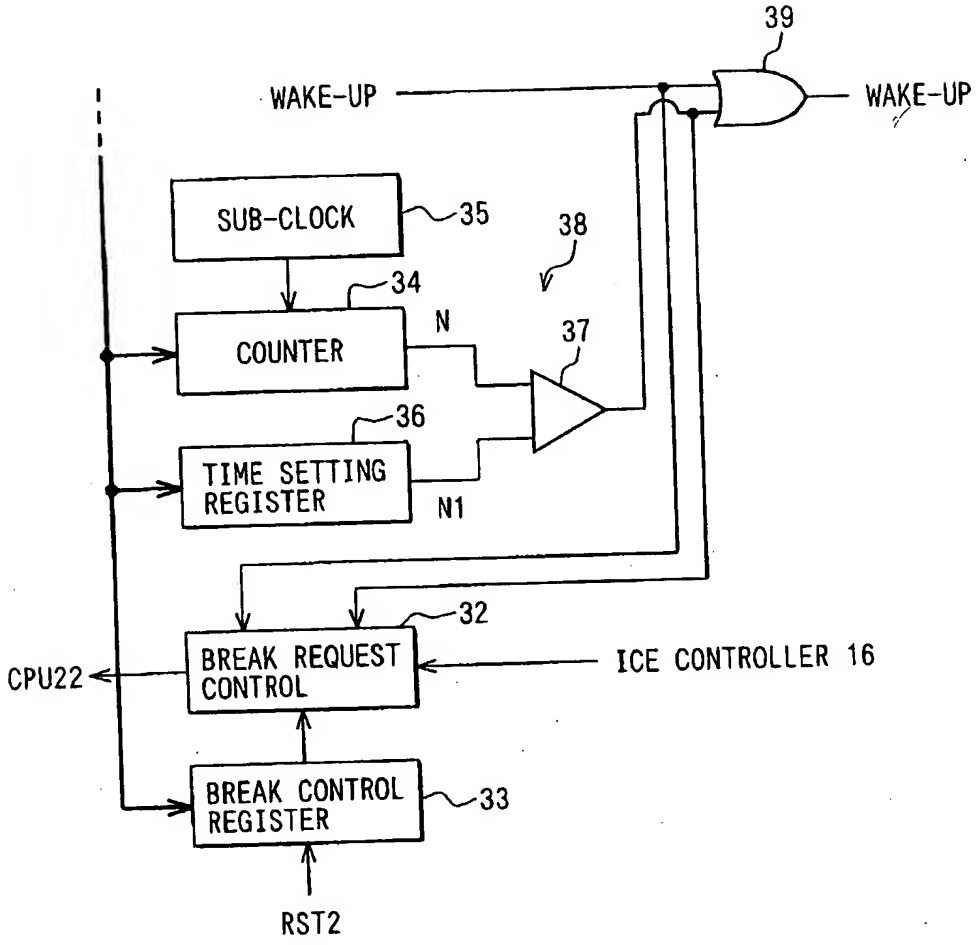

39
WAKE-UP
WAKE-UP
SUB-CLOCK
35
38
34
COUNTER
N
37
36
TIME SETTING REGISTER
N1
32
CPU22
BREAK REQUEST CONTROL
ICE CONTROLLER 16
BREAK CONTROL REGISTER
33
RST2

FIG. 5A

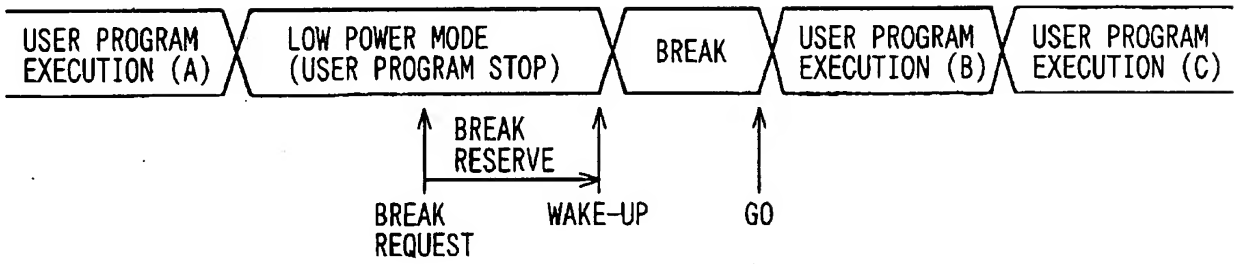

USER PROGRAM EXECUTION (A)
LOW POWER MODE (USER PROGRAM STOP)
BREAK
USER PROGRAM EXECUTION (B)
USER PROGRAM EXECUTION (C)
BREAK RESERVE
BREAK REQUEST
WAKE-UP
GO

FIG. 5B

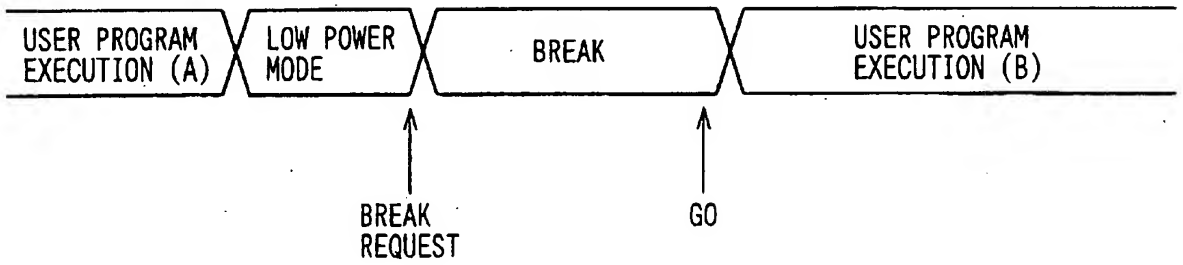

USER PROGRAM EXECUTION (A)
LOW POWER MODE
BREAK
USER PROGRAM EXECUTION (B)
BREAK REQUEST
GO

FIG. 6A

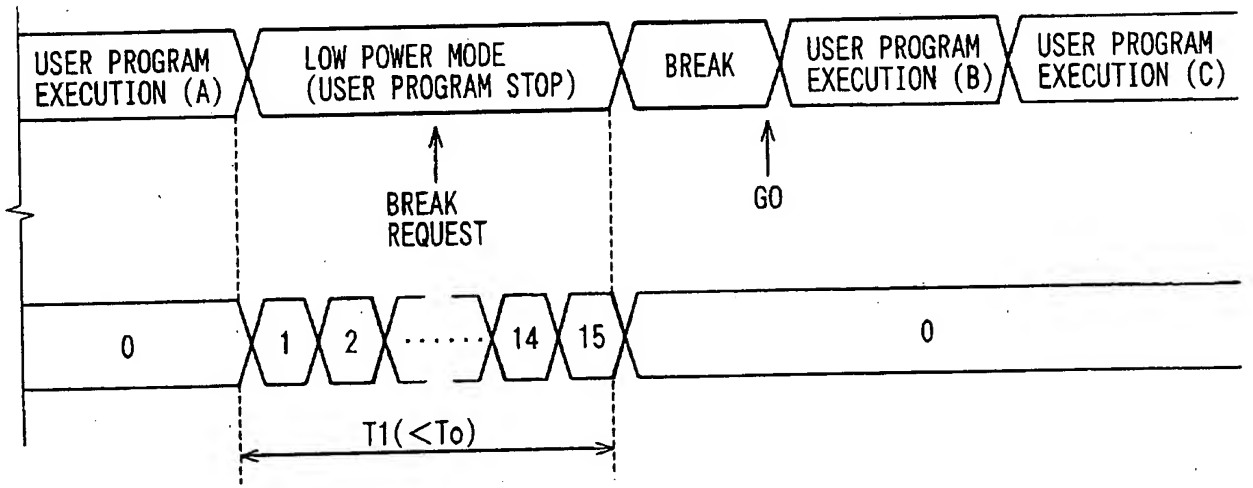
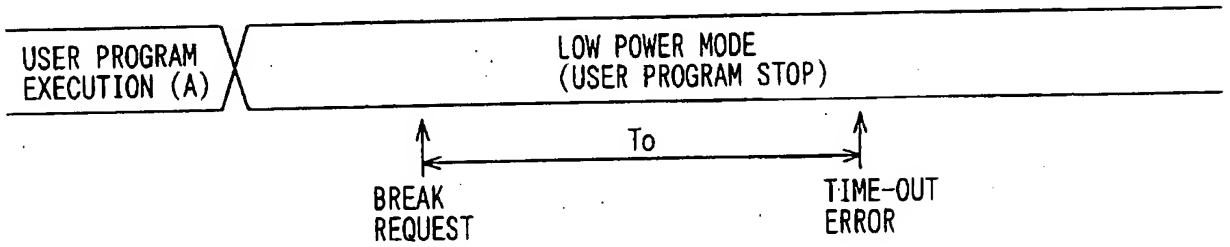

USER PROGRAM EXECUTION (A)
LOW POWER MODE (USER PROGRAM STOP)
BREAK
USER PROGRAM EXECUTION (B)
USER PROGRAM EXECUTION (C)
BREAK REQUEST
GO
0
1
2
14
15
0
T1(<To)

FIG. 6B


USER PROGRAM EXECUTION (A)
LOW POWER MODE (USER PROGRAM STOP)
To
BREAK REQUEST
TIME-OUT ERROR

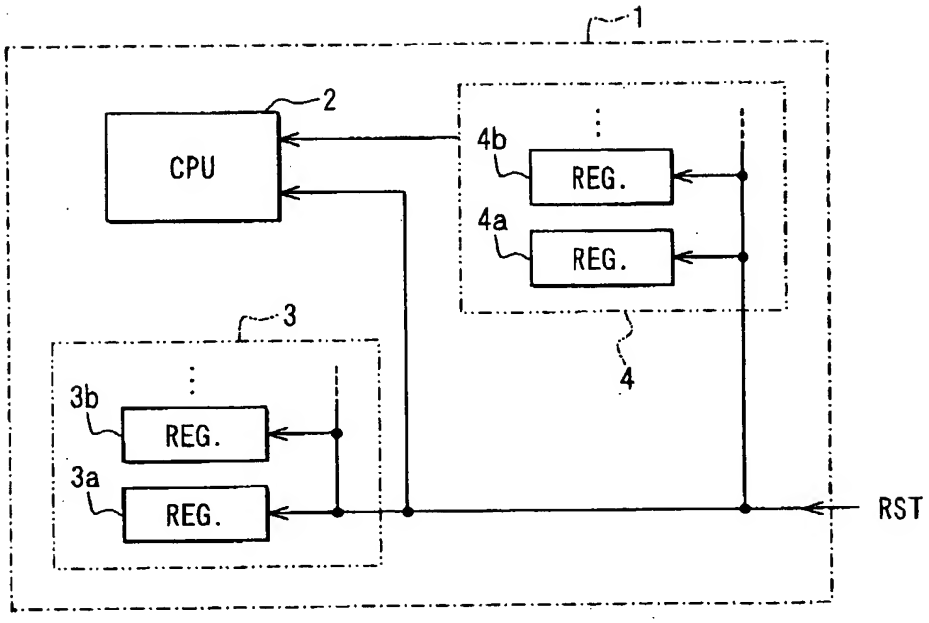



FIG. 7 PRIOR ART